it is submitted that this application is in condition for allowance.

In the Action, the examiner requires a new title of the invention because the title is not descriptive. Since the title has been amended to "SEMICONDUCTOR DEVICE HAVING WIRING PATTERNS AND DUMMY PATTERNS COVERED WITH INSULATING LAYER" as the examiner suggested in this action, Applicant believes that the objection regarding the title is no longer applicable.

In the Action, the amendment filed March 28, 2002 is objected to under 35 U.S.C. 132 because it introduces new matter. The added material is "wherein the edge of the insulating layer is located on the pad pattern which is adjacent to the dummy pattern" referring to claim 29. Since claim 29 has been amended, Applicant believes that this objection is no longer applicable.

In the Action, claims 29-33 are rejected under 35 U. S. C. 112, first paragraph, as containing subject matter which was not described in the specification. Since claim 29 has been amended, Applicant believes that this objection is no longer applicable to claim 29. Further, since claim 33 depends from claim 29, Applicant believes that this objection is also no longer applicable to claim

33. As to claims 30-32, claims 30-32 depend from claim 1 directly or indirectly. Since none of Claim 1 and claims 30-32 contains the limitation "where the edge of the insulating layer is located on the pad pattern which is adjacent to the dummy pattern", Applicant could not understand the reasons of the rejection. Thus, Applicant respectfully requests the detail explanation of the reasons of this rejection to claims 30-32.

In the Action, claims 11, and 16-20 are rejected under 35 U. S. C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. First, since claim 11 has been amended, Applicant believes that the rejection under 35 U. S. C. 112, second paragraph regarding claim 11 is no longer applicable. As to claim 16, the examiner asserts that one pattern (fourth) cited in claim 16 can not surround any thing. Although Applicant disagrees the examiner's assertion because RANDOM HOUSE WEBSTER'S UNABRIDGED DICTIONARY, second edition, does not support the examiner's assertion, claim 16 has been amended to "the bonding pad is surrounded by the first and fourth dummy patterns". Thus, the

rejection of claim 16 under 35 U. S. C. 112, second paragraph accordingly should be withdrawn. Further, since claims 17-20 depend from claim 16 directly or indirectly, the rejection of claims 17-20 under 35 U. S. C. 112, second paragraph also should be withdrawn.

In the Action, claims 16-20 and claims 29-33 are rejected under 35 U. S. C. 112, second paragraph, as failing to set forth the subject matter which applicant regards as the invention. The examiner asserts that evidence that claims 16-20, and 29-33 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No. 11 filed March 28, 2002. Applicant disagrees. In the Paper No. 11, Applicant explained the differences between claim 1 of the invention and the cited reference (YAMAHA et al.). In other words, the first dummy pattern is formed in the peripheral area in the invention. On the contrary , the dummy pattern 13 of YAMAHA et al. is formed in the circuit area. The Paper No. 11 does not mention the fourth dummy pattern of the invention cited in claim 16. Furthermore, there is no limitation where the fourth dummy pattern is formed in any claims. Thus, since Applicant could not understand the reasons of the rejection

regarding claims 16-20 and 29-33, Applicant respectfully requests the detail explanation of the reasons of this rejection to claims 16-20 and 29-33.

In the Action, claims 1-15 are rejected under 35 U. S. C. 103(a) as being unpatentable over Lee in view of Hosoda et al. The rejection is respectfully traversed.

As pointed out in the Paper filed March 28, 2002, the invention defined in claim 1 relates to a semiconductor device having wiring patterns and dummy patterns covered with an insulating layer. The characteristics of the invention claimed in independent claim 1 are:

(a) a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is **not** formed, the peripheral area surrounding the circuit area,

(b) a dummy pattern (202a) formed in the peripheral area, and

(c) a second insulating layer (204) being **not** formed over the dummy pattern and the second insulating layer being formed over the wiring patterns.

According to this structure, since the second insulating layer is not formed

over the dummy pattern, which is formed in the peripheral area surrounding the circuit area, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

However, Lee does not disclose the characteristics described above. The examiner asserts that a line 22 or 42 is a dummy line in the Lee reference. **This is clearly incorrect.** The reference number 42 of Lee is a dummy metal stripe 42, and a line 22 of Lee **is not** a dummy line. Please refer to paragraph 4 lines 24-25 of the Lee reference. Thus, Lee simply shows that the dummy line 42 is formed between the lines 20, 22 and that the SOG layer 48 is formed between the lines 20, 22. By forming the dummy line 42 between the lines 20, 22 of Lee, the layer 48 fills in the gaps between the lines and presents a relatively planar surface (paragraph 4 lines 41-43). Thus, Lee discloses that the dummy layer 42 is formed in the circuit area, not the peripheral area. As a result, Lee cannot avoid coming moisture into the circuit area so that one of the lines 20, 22 may be corroded by moisture. On the contrary, as described above, since a dummy layer 202a of the

invention is formed in the peripheral area surrounding the circuit area and the second insulating layer 204 is not formed over the dummy layer 202a, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area. Further, with reference to Fig. 7D, the examiner asserts that the second insulating layer of the invention is disclosed in Lee. **Applicant disagrees.** As descried above, although the second insulating layer is not formed on the dummy pattern, the second insulating layer is formed over the wiring patterns. However, Lee does not disclose the second insulating layer formed over the metal layer 20 or 22 in Fig. 7D.

As described in Paper filed March 28, 2002, Hosoda et al. disclose a plurality of dummy patterns 14 or 14a to reduce wiring capacitance. According to Hosoda et al., the dummy patterns 14 or 14a are formed between the wirings 13 or between the wiring 13 and a guard pattern 15 in order to form cavities 17 between the wiring 13 and the dummy pattern 14 when the insulating layer 16 is formed. Therefore, in the disclosure of the Hosoda et al. reference, it is required to form the insulating layer 16 on the dummy layer. Therefore, Hosoda et al. cannot avoid

coming moisture into the circuit area so that the wiring 13 may be corroded by moisture. On the contrary, according to the invention, since the second insulating layer 204 is not formed over the dummy layer 202a, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

The examiner asserts that Hosoda et al. teach that dummy pattern (14a) can be formed anywhere on a chip including surrounding the circuit pattern, hence periphery (See, Fig. 3), and that it would have been obvious to one having the skill in the art at the time of the invention to form the dummy pattern (42) of Lee surrounding the circuit pattern (20) as taught by Hosoda to improve the planarity of the chip. Applicant disagree. First, as described above, the purpose for forming the dummy pattern 202a in the peripheral area surrounding the circuit area is not the improvement of the planarity of the insulating layer near the edge of the chip. The purpose for forming the dummy pattern in the peripheral area is to avoid coming moisture into the circuit area. Thus, the second insulating layer should not be formed on the dummy layer. Further, since the dummy pattern 42 of Lee

should be formed between the lines 20 ,22, Applicant does not understand how the dummy pattern 42 of Lee encompasses the circuit area.

Therefore, since Lee and Hosoda et al. alone or in combination neither show nor suggest the characteristics (a) - (c) described above, which are defined in claim 1, claim 1 clearly is deemed to be clearly patentable over Lee in view of Hosoda et al., and the rejection of claim 1 accordingly should be withdrawn. Further, claims 2-15 depend from claim 1 directly or indirectly so that the rejection of these claims also should be withdrawn.

In the Action, the examiner further asserts that the expression "the width of the first (and third) dummy pattern is fixed by a concentration of solid content of the SOG (claims 3, 14 and 19); where a concentration of solid content of the SOG layer is around 5.2 wt% (claims 4, 10, 15 and 20); thermally planarized surface (claim5) are taken to be a product by process limitation and is given no patentable weight. Since these claims had been amended on March 28, 2002, and these claims have been further amended, Applicant believes that the examiner's assertion is no longer applicable. Specifically, in claim 3, the SOG layer and the first dummy pattern are

directly claimed, and in claims 4, 10, 14, 15, 19 and 20, the first dummy pattern and the concentration of solid content of the SOG layer are directly claimed. Thus, these claims are directed to the product per se.

As to claim 2, the examiner asserts that the second insulating layer (48) of Lee is a SOG layer. However, as described above, since claim 1 clearly is deemed to be clearly patentable, claim 2 is also deemed to be patentable.

As to claim 3, the examiner asserts that the first dummy pattern(42) of Lee has a width, which appears to be fixed by the concentration of solid content of the SOG. Applicant could not find any disclosure that the examiner pointed out. Applicant respectfully request to point out clearly where it is disclosed in Lee.

As to claim 4, the examiner asserts that the width of the first dummy pattern is designed for various size including less than 1 μm. However, as described above, since claim 1 clearly is deemed to be clearly patentable, claim 4 is also deemed to be patentable.

As to claim 5, the examiner asserts the semiconductor device of YAMAHA is substantially similar as claimed (See Fig. 12). First of all, YAMAHA does not

have Fig. 12. Further, according to the content of the examiner's assertion, the examiner might assert the semiconductor device of Lee not YAMAHA is substantially similar as claimed. Thus, the followings are differences between claim 5 and Lee. First of all. claim 5 depends from claim 1. Thus, as described above, since claim 1 clearly is deemed to be clearly patentable, claim 5 is also deemed to be patentable. Further, the examiner asserts that a second dummy pattern (44:lower) is formed under the first dummy pattern (44:upper) and a fourth insulating layer (18) is formed on the second dummy pattern (44:lower). This is not true. The fourth insulating layer (18) is not formed on the second dummy pattern (44:lower), is formed under the second dummy pattern (44:lower). Moreover, the examiner asserts that the first dummy pattern (44:upper) is formed on the fourth insulating layer (18). This is not true. The first dummy pattern (44:upper) is formed on a layer, which is formed between the dummy patterns (upper 44 and lower 44), not on the fourth insulating layer (18).

As to claims 6-15, claims 6-15 depend from claim 1 directly or indirectly. Since claim 1 clearly is deemed to be clearly patentable as described above, claims

6-15 are also deemed to be patentable. As to claim 9, the examiner asserts that the width of the first and second dummy patterns (44) of Lee appears to be fixed by the concentration of solid content of the SOG. Applicant could not find any disclosure that the examiner pointed out. Applicant respectfully request to point out clearly where it is disclosed in Lee. Further, as to claim 13, the examiner asserts that Lee teaches that the width of the line will approximately equal the spacing of the lines in areas where lines are closely spaced. Applicant could not find any disclosure that the examiner pointed out. Applicant respectfully request to point out clearly where it is disclosed in Lee.

In the Action, In the Action, claims 16 - 20 are rejected under 35 U. S. C. 103(a) as being unpatentable over Lee and Hosoda et al. as applied to claim 1, and further in view of Yang et al. The rejection is respectfully traversed.

First of all, claims 16 - 20 depend from claim 1 directly or indirectly. Thus, since, as described above, Lee and Hosoda et al. alone or in combination neither show nor suggest the characteristics (a) - (c) described above, which are defined in claim 1, specifically the characteristic that the second insulating layer is not formed

above the dummy layer. Next, as described in the Paper filed March 28, 2002, Yang et al. simply disclose that a dummy metal 34 is formed between metal lines 30, 31 for the planarization. Therefore, not only all dummy layers are formed in the circuit area, but also an insulating layer 36 is formed above the dummy layer. On the contrary, the first dummy layer of the invention is formed in the peripheral area where an integrated circuit is not formed. Therefore, in the device of Yang, it is impossible to avoid coming moisture into the circuit area. Further, the examiner asserts with reference to Fig. 3C of Yang, a fourth dummy layer surrounding bonding pad. **Applicant disagrees**. According to Fig. 3C, the dummy pattern is placed on the both side of the metal line 30 (which is not the bonding pad). According to the amended claim 16, a fourth dummy pattern is connected to the first dummy pattern and the bonding pad is surrounded by the first and fourth dummy patterns. Therefore, since Lee, Hosoda et al. and Yang et al. do not disclose neither the dummy pattern formed in the peripheral area and the second insulating layer not being formed above the dummy pattern nor the characteristics (a)-(c) described above, claim 16-20 clearly is deemed to be clearly patentable over Lee

and Hosoda et al. as applied to claim 1, and further in view of Yang et al., and the rejection of claim 16-20 accordingly should be withdrawn.

Further, Applicant could not understand the examiner's assertion at the last paragraph at page 9. The examiner asserts that with respect to "the second insulating layer being not formed on the fourth dummy pattern", the second insulating layer (48) of Lee is not formed on the metal lines, thus, fourth dummy pattern (44) is included. However, twice amended claim 1 includes the limitation "wherein the second insulating layer is formed over the wiring patterns", which is not disclosed in Lee.

As to claims 17-20, claims 17-20 depend from claim 1 indirectly. Since claim 1 clearly is deemed to be clearly patentable as described above, claims 17-20 are also deemed to be patentable.

In the Action, claims 27 and 28 are rejected under 35 U. S. C. 103(a) as being unpatentable over Yamaha et al. in view of Hosoda et al. The rejection is respectfully traversed. The invention defined in claim 1 relates to a semiconductor device having wiring patterns and dummy patterns covered with an insulating layer.

The characteristics of the invention claimed in independent claim 27 are:

(a) a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is **not** formed, the peripheral area surrounding the circuit area,

(b) a dummy pattern (202a) formed in the peripheral area, and

(c) an insulating layer (204) being **not** formed over the dummy pattern and the insulating layer being formed over the wiring patterns.

However, as described in Paper filed March 28, 2002, Yamaha et al. do not disclose the characteristics described above. That is, Yamaha et al. simply disclose a dummy pattern 13, which planarizes a insulating layer 14 on which an upper layer wiring 15 is formed. In other words, the dummy pattern 13 is formed in a region where a lower layer wiring 12 is not formed closely, **not in the peripheral area surrounding the circuit area,** in order to planarize the surface of the insulating layer 14 because the thickness of the insulating layer 14 in the region where the lower layer wiring 12 is not formed closely is different from that in a region where the lower layer wiring 12 is formed closely. Thus, Yamaha et al. disclose

that the dummy layer 13 is formed in the circuit area, not the peripheral area. As a result, Yamaha et al. cannot avoid coming moisture into the circuit area so that the lower layer wiring may be corroded by moisture. On the contrary, as described above, since a dummy layer 202a of the invention is formed in the peripheral area surrounding the circuit area and the second insulating layer 204 is not formed over the dummy layer 202a, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

Further, the examiner asserts that Yamaha et al. disclose a dummy area (RB) in Fig. 5. Applicant disagrees. The area (RB) in Fig. 5 is a part of the circuit area but the peripheral area because an upper layer wiring 16, which is a part of an active circuit, is formed over the dummy layer 13. Thus, the area (RB) simply shows the region where the lower layer wiring 12 is not formed closely.

Moreover, Yamaha et al. disclose in the paragraph [0017] of Japanese laid open patent 10-270445 written in Japanese that there is the thin SOG insulating layer on the dummy pattern. This is quite different structure from that of the

invention.

Hosoda et al. disclose a plurality of dummy patterns 14 or 14a to reduce wiring capacitance. According to Hosoda et al., the dummy patterns 14 or 14a are formed between the wirings 13 or between the wiring 13 and a guard pattern 15 in order to form cavities 17 between the wiring 13 and the dummy pattern 14 when the insulating layer 16 is formed. Therefore, in the disclosure of the Hosoda et al. reference, it is required to form the insulating layer 16 on the dummy layer. Therefore, Hosoda et al. cannot avoid coming moisture into the circuit area so that the wiring 13 may be corroded by moisture. On the contrary, according to the invention, since the insulating layer 204 having a moisture absorbable characteristic is not formed over the dummy layer 202a, moisture cannot come into the circuit area through the insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

The examiner asserts that Hosoda et al. teach that dummy pattern (14a) can be formed anywhere on a chip including surrounding the circuit pattern at the edge of the chip and that it would have been obvious to one having the skill in the

art at the time of the invention to form the dummy pattern (13) of Yamaha et al. surrounding the circuit pattern (12s) as taught by Hosoda to improve the planarity of the insulating layer near the edge of the chip. Applicant disagree. First, as described above, the purpose for forming the dummy pattern 202a in the peripheral area surrounding the circuit area is not the improvement of the planarity of the insulating layer near the edge of the chip. The purpose for forming the dummy pattern in the peripheral area is to avoid coming moisture into the circuit area. Thus, the insulating layer having a moisture absorbable characteristic should not be formed on the dummy layer. Further, even if the dummy pattern 13 of Yamaha et al. surrounds the circuit pattern as taught by Hosoda, it is not possible to avoid coming moisture into the circuit area because the insulating layer 14b of Yamaha et al. is formed on the dummy pattern 13.

Therefore, since Yamaha et al. and Hosoda et al. alone or in combination neither show nor suggest the characteristics (a) - (c) described above, which are defined in claim 27, claim 27 clearly is deemed to be clearly patentable over Yamaha et al. in view of Hosoda et al., and the rejection of claim 27 accordingly

should be withdrawn. Further, claims 28 depend from claim 27 directly so that the rejection of claim 28 also should be withdrawn.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any further fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Attached hereto is a marked-up version of the changes made to the, title, specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the title of the invention

The title of the invention has been twice amended as follows:

SEMICONDUCTOR DEVICE HAVING WIRING PATTERNS AND DUMMY PATTERNS COVERED WITH INSULATING LAYER

In the specification

Paragraph beginning at line 2 of page 14 has been amended as follows:

The fourth embodiment is described below with reference to Fig. 6 ~~7~~. Referring to Fig. 6 ~~7~~, a pair of inner and outer dummy patterns 500a, 500b (a third dummy pattern and a first dummy pattern) are formed in the dummy area. Each dummy pattern has a same width (Lw), and formed in the same method with the same size described in the first embodiment. The length (Ls2) between the dummy patterns 500a, 500b is designed for over 0.9 μm.

Paragraph beginning at line 15 of page 14 has been amended as follows:

The fifth embodiment is described below with reference to Figs. 7A and 7B. A bonding pad 601 is formed in a circuit area, and an outer dummy pattern 600b ~~600a~~ (a first dummy pattern) is formed in a dummy area. The size, location and manufacturing process of the outer dummy pattern is the same as the dummy pattern described in the first embodiment. That is, a width of the outer dummy pattern is designed for 1 μm, and the length (L) is designed for 10 μm. A frame-shaped fourth dummy pattern 600a ~~600b~~ is formed for surrounding the bonding pad 601 in the circuit area. The distance (Ls3) between the bonding pad 601 and the fourth dummy pattern 600a ~~600b~~ or the outer dummy pattern 600b ~~600a~~ is designed for over 0.9 μm. The distance (Ls1) between the metalized wiring pattern 600 and ~~the outer dummy pattern 600a or~~ the fourth dummy pattern 600a is designed for over 0.5 μm because of the same reason described in the first embodiment. The metalized wiring pattern 600, the outer dummy pattern 600b and the fourth dummy pattern 600a are formed simultaneously by etching a conductive layer.

In the claims:

Claims 1, 3, 4, 9-11, 13-16, 18-20, 27, 29, and 31-33 have been amended as follows.

1 (2nd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is not formed, the peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on the circuit area and the peripheral area of the semiconductor substrate;

a second insulating layer formed on the first insulating layer which is formed on the semiconductor substrate, wherein the second insulating layer is formed over the wiring patterns, and the second insulating layer is not formed over the first dummy pattern; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

3 (2nd amended). A semiconductor device as claimed in claim 2, wherein

the SOG layer has a certain concentration of solid content, and the first dummy pattern has a width, which is determined ~~fixed~~ by the ~~a~~ concentration of solid content of the SOG layer.

4 (2nd amended). A semiconductor device as claimed in claim 2 ~~1~~, wherein the first dummy pattern has a width, which is ~~designed for~~ less than 1 μm, and ~~where~~ a concentration of solid content of the SOG layer is around 5.2 wt%.

9 (1st amended). A semiconductor device as claimed in claim 8 ~~6~~, wherein the SOG layer has a certain concentration of solid content, and each of ~~the widths of~~ the first and second dummy patterns has a width, which is determined ~~are fixed~~ by the a concentration of solid content of the SOG.

10 (2nd amended). A semiconductor device as claimed in claim 8 ~~6~~, wherein each of the first and second dummy patterns has a width, which is ~~designed for~~ less than 1 μm, and ~~where~~ a concentration of solid content of the SOG layer is around 5.2 wt%.

11 (2nd amended). A semiconductor device as claimed in claim 1, further comprising:

a third dummy pattern formed in the peripheral area between the first

dummy pattern and the wiring patterns, the second ~~first~~ insulating layer being not formed on the third dummy pattern.

13 (2nd amended). A semiconductor device as claimed in claim 11, wherein the distance between the first dummy pattern and the third dummy pattern exceeds ~~is designed for over~~ 0.9 μm.

14 (2nd amended). A semiconductor device as claimed in claim 11 ~~12~~, wherein the second insulating layer is a SOG layer, the SOG layer has a certain concentration of solid content, and each of the first and third dummy layer has a width, which is determined ~~fixed~~ by the ~~a~~ concentration of solid content of the SOG layer.

15 (2nd amended). A semiconductor device as claimed in claim 11 ~~12~~, wherein the second insulating layer is a SOG layer, each of the first and third dummy layer has a width, which is ~~designed for~~ less than 1 μm, and ~~where~~ a concentration of solid content of the SOG layer is around 5.2 wt%.

16 (2nd amended). A semiconductor device as claimed in claim 1, further comprising:

a bonding pad formed on the semiconductor substrate in the circuit area; and

a fourth dummy pattern, which is connected to the first dummy pattern ~~surrounding the bonding pad~~, the second insulating layer being not formed on the fourth dummy layer,

wherein the bonding pad is surrounded by the first and fourth dummy patterns.

18 (1st amended). A semiconductor device as claimed in claim 16, wherein a distance between the fourth dummy pattern and the bonding pad exceeds ~~is designed for over~~ 0.9 μm.

19 (2nd amended). A semiconductor device as claimed in claim 16 ~~17~~, wherein the second insulating layer is a SOG layer, the SOG layer has a certain concentration of solid content, and each of the first and fourth dummy layer has a width, which is determined ~~fixed~~ by the ~~a~~ concentration of solid content of the SOG layer

20 (2nd amended). A semiconductor device as claimed in claim 16 ~~17~~, wherein each of the first and fourth dummy layer has a width, which is ~~designed for~~ less than 1 μm, and ~~where~~ a concentration of solid content of the SOG layer is around 5.2 wt%.

27 (1st amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is not formed, the peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area; and

an insulating layer formed above the semiconductor substrate, the insulating layer being formed over the wiring patterns, the insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern, and the insulating layer having a moisture absorbable characteristic.

29 (1st amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is not formed, the peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area, the wiring pattern including a pad pattern;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

~~and~~

a first insulating layer formed over the wiring patterns and the dummy pattern, an edge of the first insulating layer being located on the pad pattern, which is adjacent the dummy pattern; and

a second ~~an~~ insulating layer formed above the semiconductor substrate, the second insulating layer being formed over the wiring patterns and the second insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern~~,~~

~~wherein the edge of the insulating layer is located on the pad pattern which is adjacent to the dummy pattern~~.

31 (1st amended). A semiconductor device as claimed in claim 1, wherein the wiring patterns include a pad pattern, the edge of the first ~~second~~ insulating layer being located on the pad pattern which is adjacent to the dummy pattern.

32 (1st amended). A semiconductor device as claimed in claim 30, wherein the wiring patterns include a pad pattern, the edge of the first ~~second~~ insulating layer being located on the pad pattern which is adjacent to the dummy pattern.

33 (1st amended). A semiconductor device as claimed in claim 29, wherein the second insulating layer has a moisture absorbable characteristic.